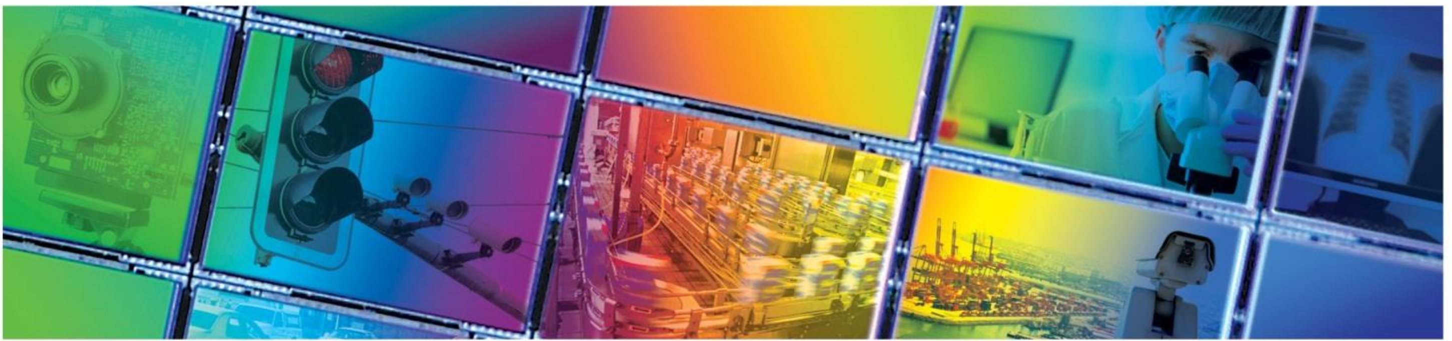
ON Semiconductor®

KAF-18500 IMAGE SENSOR

5270 (H) X 3516 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 24, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0074

TABLE OF CONTENTS

Summary Specification **4**
Description 4
Features 4
Applications 4
Ordering Information **5**
Device Description **6**
Architecture 6
Dark Reference Pixels 7
Dummy Pixels 7
Active Buffer Pixels 7
Image Acquisition 7
Charge Transport 7
Horizontal Register 8
Output Structure 8
Output Load 9
Physical Description 10
Pin Description and Device Orientation 10
Imaging Performance **12**
Typical Operational Conditions 12
Specifications 12
Typical Performance Curves **14**
Defect Definitions **16**
Operating Conditions 16
Specifications 16
Operation **17**
Absolute Maximum Ratings 17
Power-up Sequence 17
DC BIAS Operating Conditions 18
AC Operating Conditions 18
Clock Levels 18
Timing **19**
Requirements and Characteristics 19
Edge Alignment 20
Frame Timing 21
Frame Timing Detail 21
Line TIMING (each output) 22
Pixel Timing 23
Pixel Timing Detail 24
MODE OF OPERATION **25**
Power-up Flush Cycle 25
Storage and Handling **26**
Storage Conditions 26
ESD 26
Cover Glass Care and Cleanliness 26
Environmental Exposure 26
Soldering Recommendations 26
Mechanical Information **27**
Completed Assembly 27

Cover Glass Specification 28
MAR Coated-IR Absorbing Cover Glass 28
Quality Assurance and Reliability 29
Quality and Reliability 29
Replacement 29
Liability of the Supplier 29
Liability of the Customer 29
Test Data Retention 29
Mechanical 29
Life Support Applications Policy 29
Revision Changes 30
MTD/PS-1412 30
PS-0074 30

TABLE OF FIGURES

Figure 1: Block Diagram 6
Figure 2: Output Architecture (Left or Right) 8
Figure 3: Typical Output Structure Load Diagram 9
Figure 4: Pinout Diagram - Top View 10
Figure 5: Typical Quantum Efficiency 14
Figure 6: Typical GR-GB QE Difference 14
Figure 7: Typical Normalized Angle QE 15
Figure 8: Typical Anti Blooming Performance 15
Figure 9: Timing Edge Alignment 20
Figure 10: Frame Timing 21
Figure 11: Frame Timing Detail 21
Figure 12: Line Timing 22
Figure 13: Pixel Timing 23
Figure 14: Pixel Timing Detail 24
Figure 15: Power-up Flush Cycle 25
Figure 16: Completed Assembly Drawing 27
Figure 17: Cover Glass Substrate Transmission 28

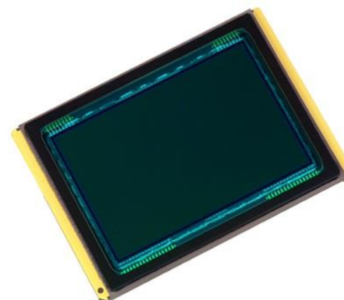
Summary Specification

KAF-18500 Image Sensor

DESCRIPTION

The KAF-18500 is a dual output, high performance color CCD (charge coupled device) image sensor with 5270 (H) x 3516 (V) photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.8 μm square pixels are selectively covered with red, green or blue pigmented filters for color separation. Microlenses are added for improved sensitivity.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.



Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	5422 (H) x 3610 (V) = 19.6 M
Number of Effective Pixels	5310 (H) x 3556 (V) = 18.8 M
Number of Active Pixels	5270 (H) x 3516 (V) = 18.5 M
Pixel Size	6.8 μm (H) x 6.8 μm (V)
Imager Size	43.1 mm (diagonal)
Chip Size	37.8 mm (H) x 26.4 mm (V)
Aspect Ratio	3:2
Saturation Signal	42 ke$^-$
Charge to Voltage Conversion	25 μV/e$^-$
Quantum Efficiency (RGB)	30%, 45%, 40%
Read Noise (f = 24 MHz)	15.7 e$^-$
Dark Signal (T = 60 °C)	50pA/cm^2
Dark Current Doubling Temperature	5.3 °C
Linear Dynamic Range (f = 24 MHz, T = 60 °C)	68.1 dB
Charge Transfer Efficiency (HCTE/VCTE)	0.999995 0.999998
Blooming Protection (4 ms exposure time)	5600X saturation exposure
Maximum Data Rate	24 MHz
Readout Mode	Dual output only
Package	PGA
Cover Glass	AR coated (S8612)

Unless noted, all parameters above are specified at T = 20 °C to 25 °C

FEATURES

- TRUESENSE Transparent Gate Electrode for high sensitivity
- High resolution, 35 mm format
- Broad dynamic range
- Low noise
- Large image area

APPLICATIONS

- Digital Still Cameras

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H2058	KAF-18500-NXA-JH-AA-08	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass , 0.8 mm glass	KAF-18500-NXA-08
4H2059	KAF-18500-NXA-JH-AE-08	Special Color, Aperture, Enhanced, ESD, LOD, Microlens, Sealed IR Cover Glass , 0.8 mm glass [Engineering Grade]	KAF-18500-NXA-08

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Device Description

ARCHITECTURE

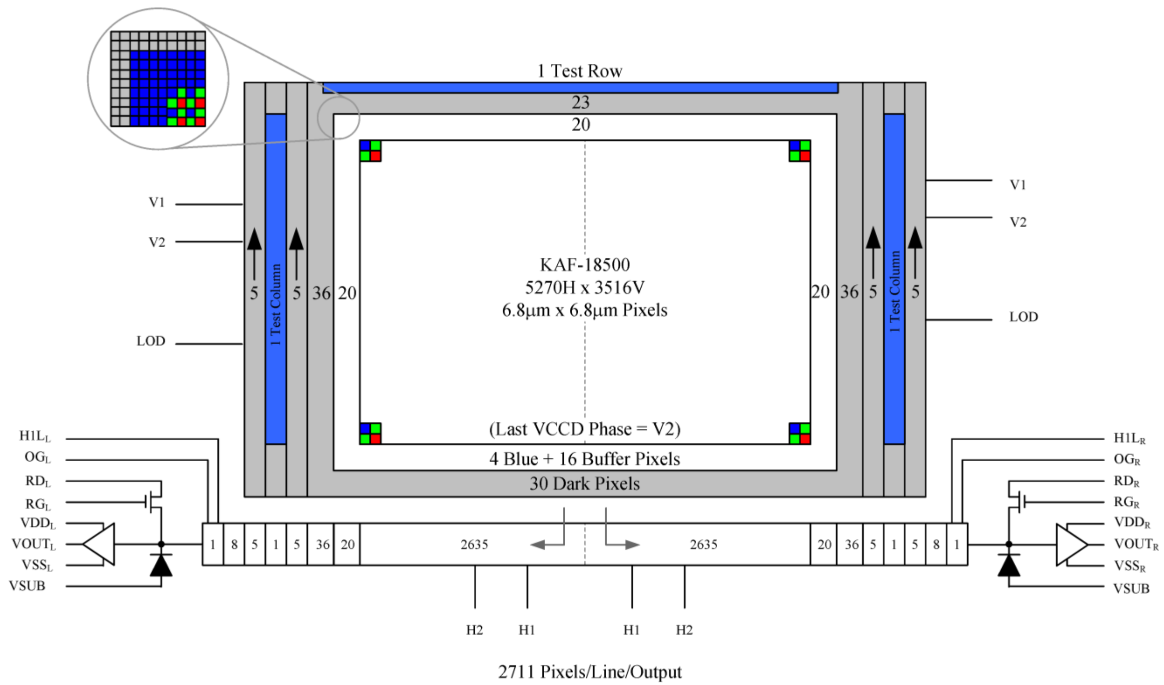


Figure 1: Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 36 leading dark pixels on every line. There are also 30 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Dummy Pixels

Within each horizontal shift register there are 20 leading additional shift phases required before the dark reference pixels: (1 + 8 + 5 + 1 + 5) (See Figure 1). These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 20 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non-uniformities. For the leading 20 active column pixels, the first 4 pixels are covered with blue pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B).

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or ‘blooming’. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each photogate (pixel) is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD’s to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented with a new line on the falling edge of V2 while H1 is held high. The horizontal CCD’s then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the floating diffusion output amplifier. On each falling edge of H1L a new charge packet is dumped onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

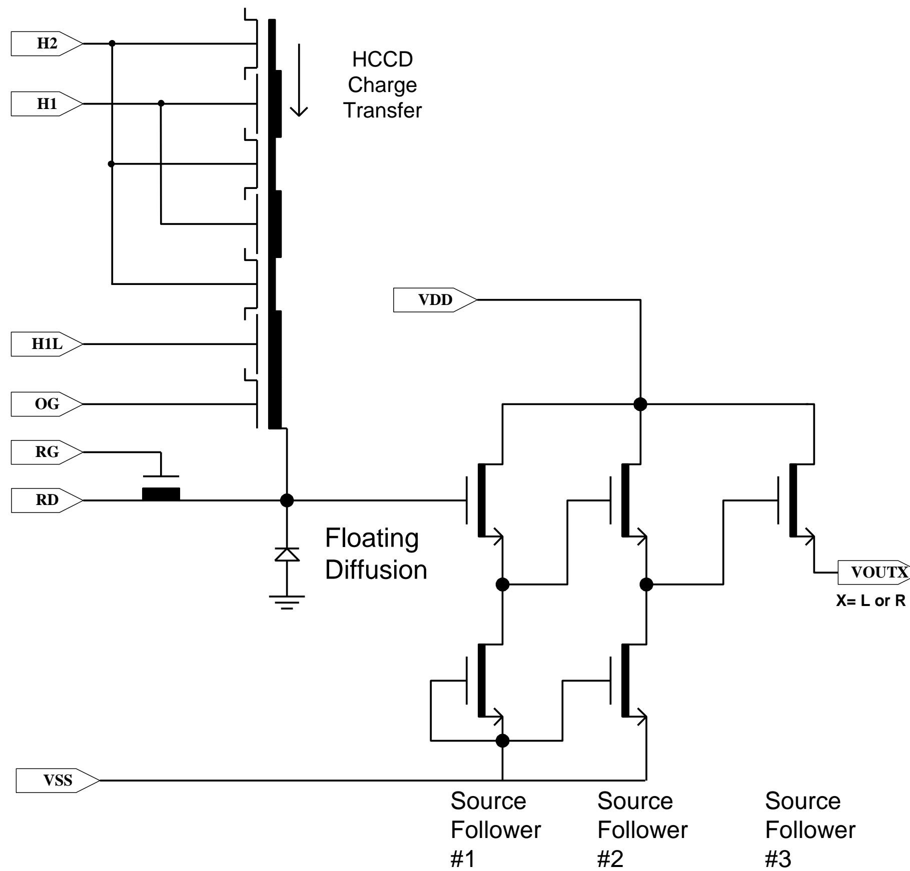


Figure 2: Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structures, an off-chip current source must be added to the VOUT pins of the device. See Figure 3.

Output Load

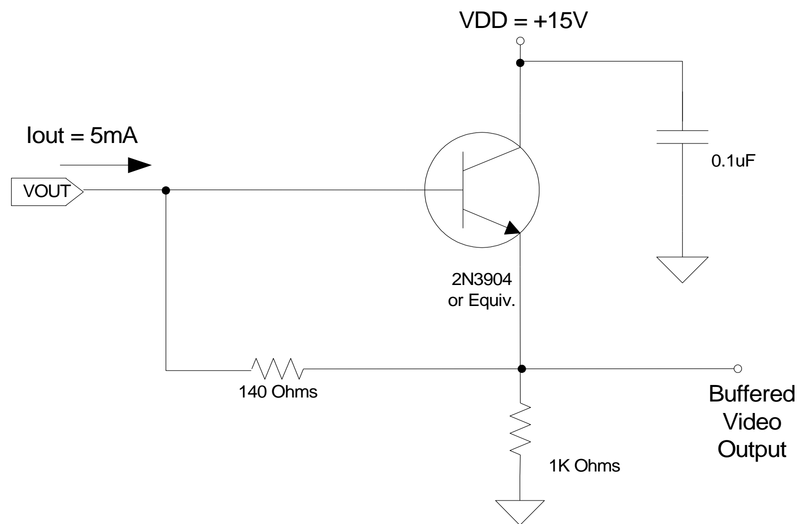


Figure 3: Typical Output Structure Load Diagram

Note: Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

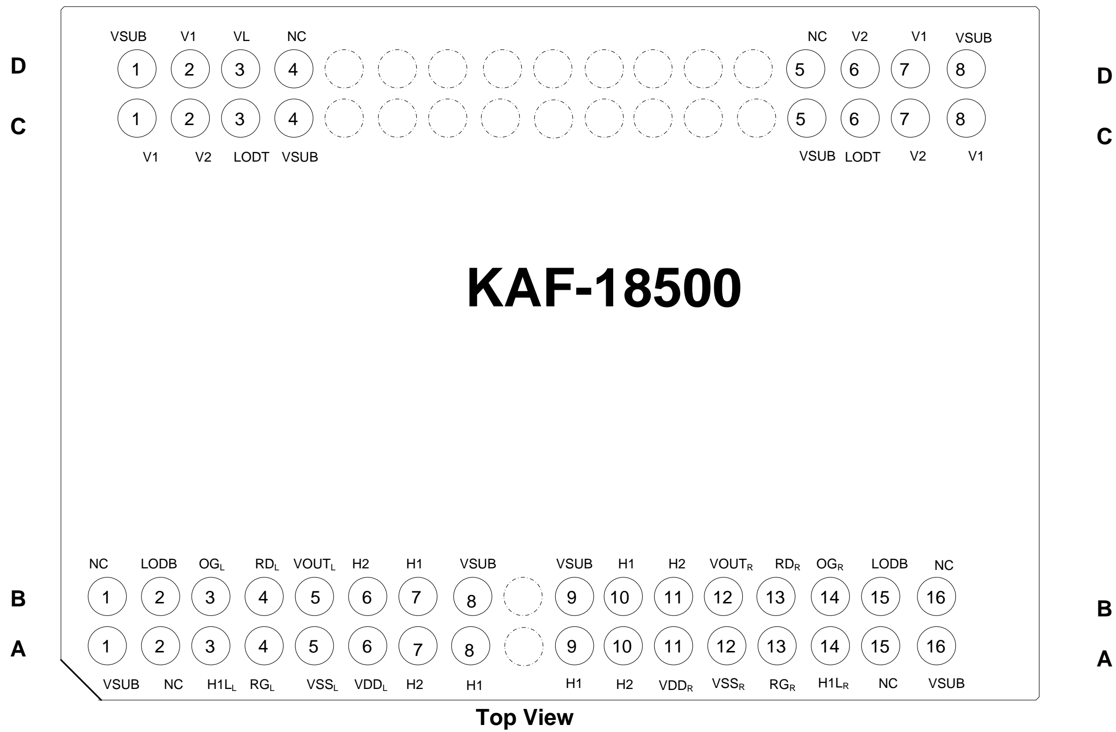


Figure 4: Pinout Diagram - Top View

PGA Grid Row A		
Pin	**Name**	**Description**
1	VSUB	Substrate
2	NC	Physical pin with no connection on die
3	$H1L_L$	Horizontal Phase 1, last phase, left side
4	RG_L	Reset Drain, left side
5	VSS_L	Output Amplifier Return, left side
6	VDD_L	Output Amplifier Supply, left side
7	H2	Horizontal Phase 2
8	H1	Horizontal Phase 1
9	H1	Horizontal Phase 1
10	H2	Horizontal Phase 2
11	VDD_R	Output Amplifier Supply, right side
12	VSS_R	Output Amplifier Return, right side
13	RG_R	Reset Gate, right side
14	$H1L_R$	Horizontal Phase 1, last phase, right side
15	NC	Physical pin with no connection on die
16	VSUB	Substrate

PGA Grid Row B		
Pin	**Name**	**Description**
1	N/C	Physical Pin with No Connection on Die
2	LODB	Lateral Overflow Drain, bottom
3	OG_L	Output Gate, left side
4	RD_L	Reset Gate, left side
5	$VOUT_L$	Video Output: left side
6	H2	Horizontal Phase 2
7	H1	Horizontal Phase 1
8	VSUB	Substrate
9	VSUB	Substrate
10	H1	Horizontal Phase 1
11	H2	Horizontal Phase 2
12	$VOUT_R$	Video Output: right side
13	RD_R	Reset Drain, right side
14	OG_R	Output Gate, right side
15	LODB	Lateral Overflow Drain, bottom
16	N/C	Physical Pin with No Connection on Die

PGA Grid Row C		
Pin	**Name**	**Description**
1	V1	Vertical Phase 1
2	V2	Vertical Phase 2
3	LODT	Lateral Overflow Drain, top
4	VSUB	Substrate
5	VSUB	Substrate
6	LODT	Lateral Overflow Drain, top
7	V2	Vertical Phase 2
8	V1	Vertical Phase 1

PGA Grid Row D		
Pin	**Name**	**Description**
1	VSUB	Substrate
2	V1	Vertical Phase 1
3	V2	Vertical Phase 2
4	N/C	Physical Pin with No Connection on Die
5	N/C	Physical Pin with No Connection on Die
6	V2	Vertical Phase 2
7	V1	Vertical Phase 1
8	VSUB	Substrate

Imaging Performance

Typical Operational Conditions

Description	Condition	Notes
Frame Time ($t_{readout}$ + t_{int})	Varies, see below	Includes overclock pixels
Readout time ($t_{readout}$)	527 ms	
Integration time (t_{int})	Varies per test: Bright Field 250 ms, Dark Field 1 sec, Saturation 250 ms, Low light 33 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 – 25 °C	Room temperature
Mode	Integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{VW} = 11 μs	

Specifications

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal	Vsat Ne^{-}_{sat} Q/V	900 (35000)	1086 42,000 25.6		mV e^{-} μV/e^{-}	1, 19	die[17] design[18] design[18]
Peak Quantum Efficiency red green blue	Rr Rg Rb		30 45 40		% % %		design[18] design[18] design[18]
High Level Photoresponse Non-Linearity	Le_High		2	10	%	2	die[17]
Low Level Photoresponse Non-Linearity	Le_Low		2	10	%	2	die[17]
Photo Response Non-Uniformity each color plane	PRNU		4.5	25	%p-p	3	die[17]
Integration Dark Signal	Vdark,int		4	10	mV/s	4,16	die[17]
Readout Dark Signal	Vdark,read		12	20	mV/s	15,16	die[17]
Dark Signal Non-Uniformity	DSNU		0.5	4	mV p-p	5	die[17]
Dark Signal Doubling Temperature	ΔT		5.3		°C		design[18]
Read Noise	N_R		15.7		e^{-} rms		design[18]
Total Noise	N		18.9		e^{-} rms	6	design[18]
Linear Dynamic Range	DR		68.1		dB	7	design[18]
Red-Green Hue Shift Blue-Green Hue Shift	RGHueUnif BGHueUnif		1.8	12	%	8	die[17]
Horizontal Charge Transfer Efficiency	HCTE	0.999995	0.999995			9	die[17]
Vertical Charge Transfer Efficiency	VCTE	0.999999	0.999998				die[17]
Blooming Protection	Xab		5600		x Vsat	10	design[18]
DC Offset, output amplifier	Vodc	6.0	8	9.5	V	11	die[17]
Output Amplifier Bandwidth	f_{-3dB}		232		MHz	12	design[18]
Output Impedance, Amplifier	R_{OUT}	100	137	300	Ohms		die[17]
Hclk Feedthru	V_{hft}		3.7	20	mV	13	die[17]
Reset Feedthru	V_{rft}		0.5		V	14	design[18]

Notes:

1. Increasing output load currents to improve bandwidth will decrease the conversion factor (Q/V).
2. Worst-case deviation (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 85% of Vsat min.
3. Difference between the maximum and minimum average signal levels of 148 x 148 blocks within the sensor on a per color basis as a % of average signal level.
4. T = 60 °C. Average non-illuminated signal with respect to over-clocked vertical register signal.
5. T = 60 °C. Absolute difference between the maximum and minimum average signal levels of 148 x 148 blocks within the sensor.
6. rms deviation of a multi-sampled pixel measured in the dark including amplifier and system noise sources.
7. 20log (0.95*Vsat/VN). Specified at T = 60 °C.
8. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (148 x 148 blocks) within the sensor.
9. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 24 MHz.
10. Xab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4 ms.
11. Video level offset with respect to ground.
12. Last stage only. Assumes 5 pF off-chip load.
13. Amount of artificial signal due to H1 coupling.
14. Amplitude of feedthrough pulse in VOUT due to RG coupling.
15. T = 60 °C. Average non-illuminated signal collected due to the read out time.
16. Total dark signal = (Vdark,int x t_{int}) + (Vdark,read x $t_{readout}$).
17. A parameter that is measured on every sensor during production testing.
18. A parameter that is quantified during the design verification activity.
19. Specified at T = 60 °C.

Typical Performance Curves

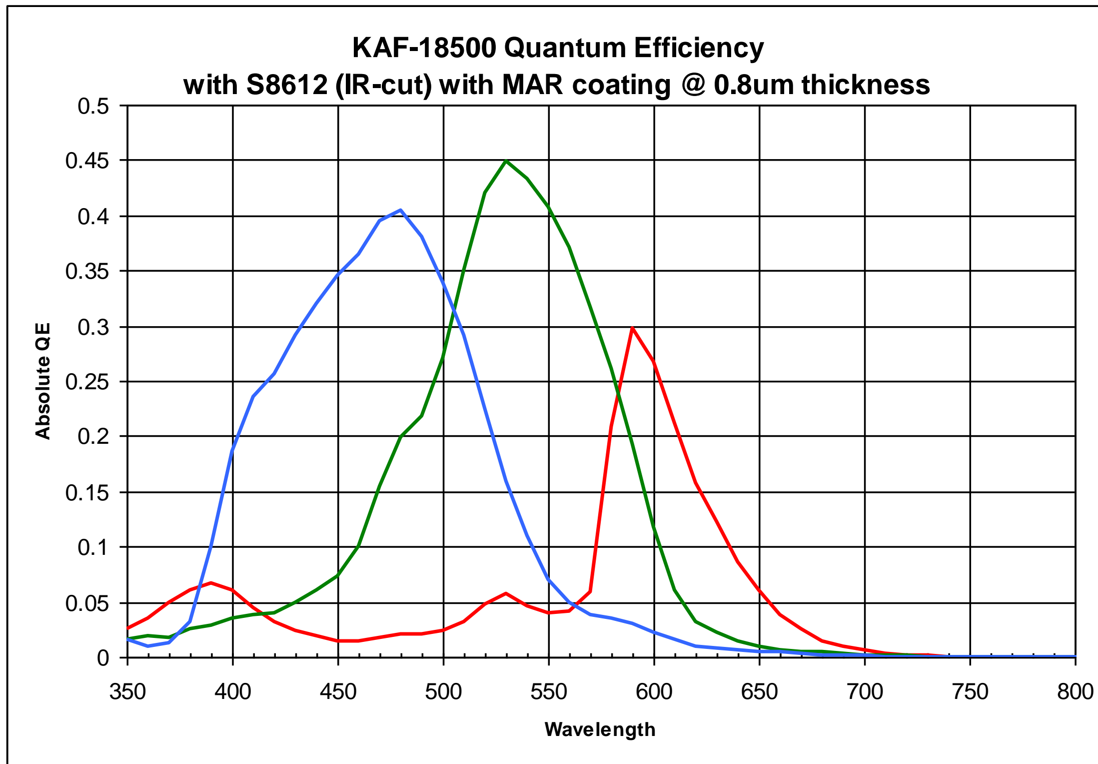


Figure 5: Typical Quantum Efficiency

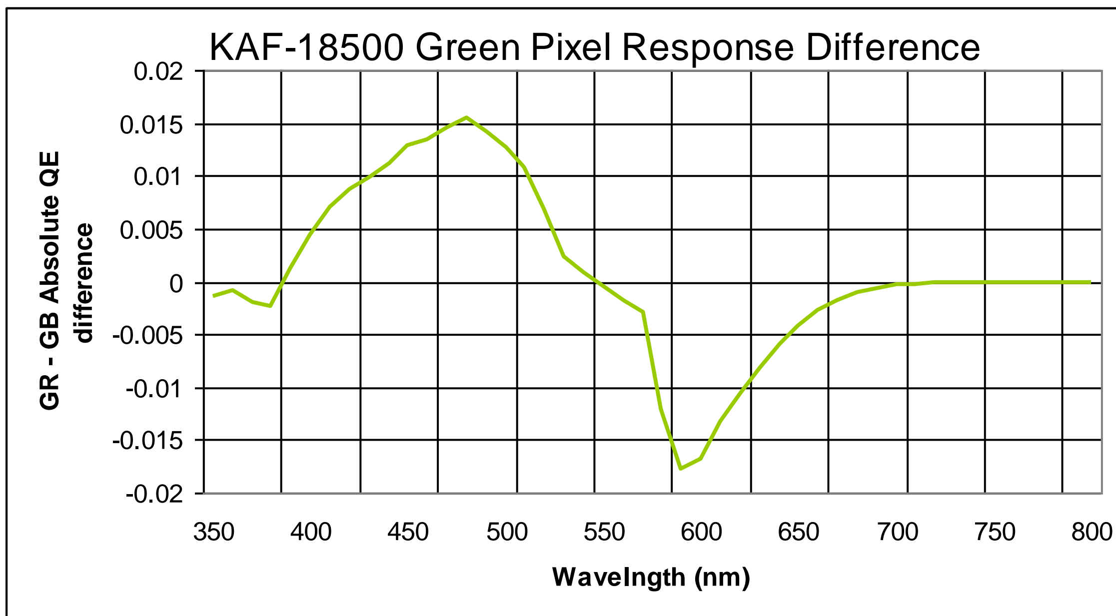


Figure 6: Typical GR-GB QE Difference

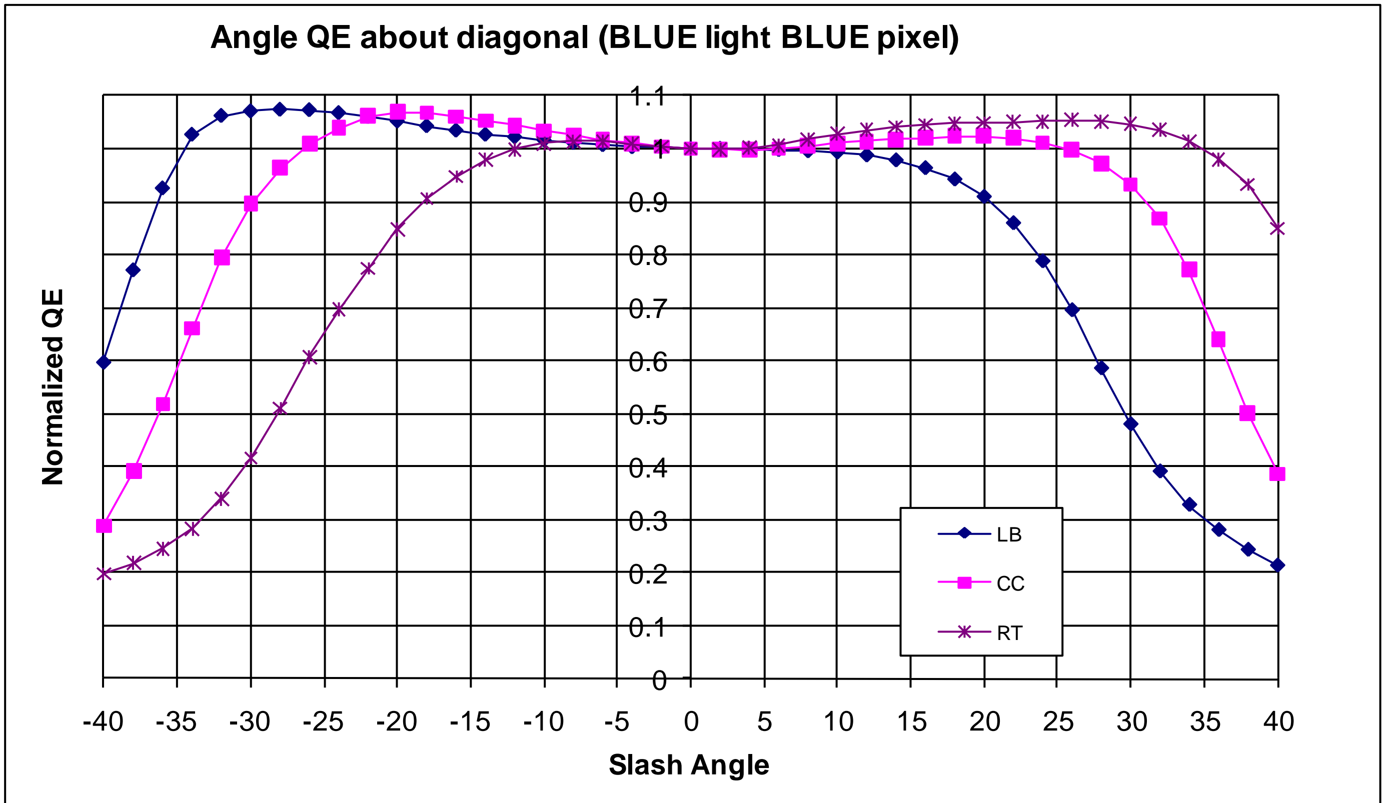


Figure 7: Typical Normalized Angle QE

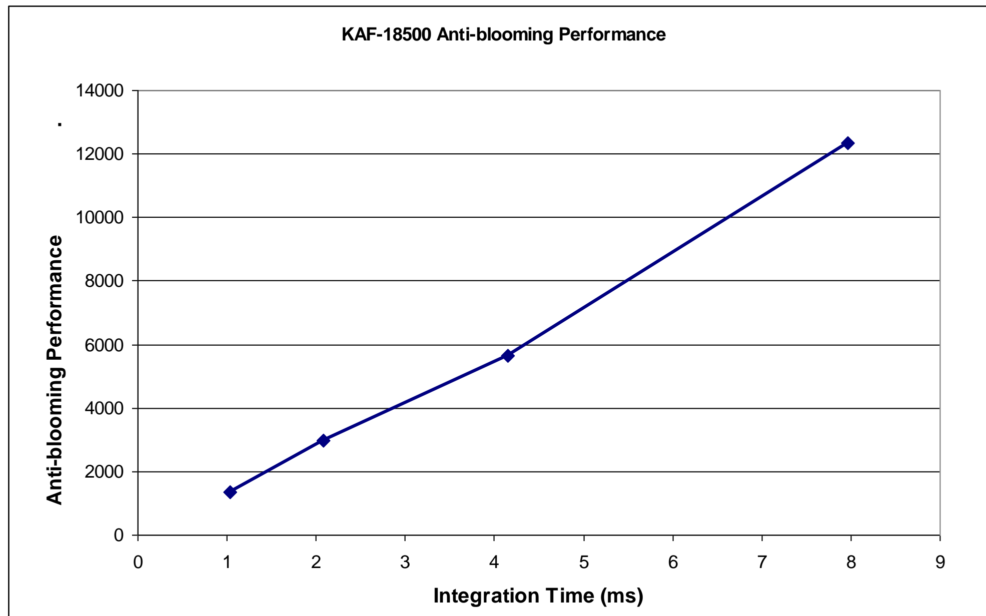


Figure 8: Typical Anti Blooming Performance

Defect Definitions

Operating Conditions

All defect tests performed at:

Description	Condition	Notes
Integration time (t_{int})	Varies per test: Bright Field 250 ms, Dark Field 1 sec, Saturation 250 ms, Low light 33 ms	
Horizontal clock frequency	24 MHz	
Temperature	20 – 25 °C	Room temperature

Specifications

Classification	Points	Clusters, small and large	Clusters, large	Columns	Includes dead columns
Standard Grade	≤ 4,400	≤ 50	≤ 5	≤ 15	yes

Point Defects A pixel that deviates by more than 9 mV above neighboring pixels under non-illuminated conditions.

-- OR --

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions.

Cluster Defect Small clusters: A grouping of adjacent point defects that can number in size from 2 to 10 pixels. Large clusters: A grouping of more than 10 pixels but not larger than 20 adjacent point defects. A single large cluster is not to exceed 5 adjacent pixels within the same color plane.

Cluster Separation Cluster defects are separated by no less than 4 good pixels in any direction .

Column Defect A grouping of more than 10 point defects along a single column.

-- OR --

A column that deviates by more than 0.9 mV above or below neighboring columns under non-illuminated conditions.

-- OR --

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions.

Column and cluster defects are separated by at least 4 good columns in the x direction. No multiple column defects (double or more) will be permitted.

Dead Columns A column that deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns A column that deviates by more than 100 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	-0.5	+17.5	V	1,2
Gate Pin Voltages	Vgate1	-13.5	+13.5	V	1,3
Gate - Gate Voltages	V1-2	-13.5	+13.5	V	4,5
Output Bias Current	Iout		-30	mA	6
LOD Diode Voltage	VLODT	-0.5	+13.0	V	7
Operating Temperature	TOP	0	60	°C	8

Notes:

1. Referenced to pin SUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, OG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to OG; V1 to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, OG to H2. These inputs contain an ESD protection circuit. Exceeding the maximum voltages will cause an uncontrolled current to flow in these circuits and may damage the input pin.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at the maximum values will reduce Mean Time to Failure (MTTF).
7. V1, H1, V2, H2, H1L, OG, and RD are tied to 0 V.
8. Noise performance will degrade at higher temperatures.
9. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.

Power-up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

a. Connect the ground pins (SUB).

b. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	RD	11.3	11.5	11.7	V	IRD = 0.01	
Output Amplifier Return	VSS	0.5	0.7	1.0	V	ISS = 3.0	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	IOUT + ISS	
Substrate	SUB		0		V	0.01	
Output Gate	OG	-2.2	-2.0	-1.8	V	0.01	
Lateral Drain	LOD	9.8	10.0	10.2	V	0.01	
Video Output Current	IOUT		-5	-10	mA		1

Notes:
1. An output load sink must be applied to VOUT to activate output amplifier - see Figure 3.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	245 nF	1.2
V1 High Level	V1H	High	2.3	2.5	2.7			
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	303 nF	1,2
V2 High Level	V2H	High	2.3	2.5	2.7			
H1, H2 (amplitude)	H1amp H2amp	Amplitude	6.5	6.75	7.0	V	See below	
H1 Low Level	H1Low	Low	-4.7	-4.5	-4.3	V	460 pF	1
H2 Low Level	H2Llow	Low	-5.2	-5.0	-4.8	V	302 pF	1
H1L Low Level	H1Llow	Low	-6.7	-6.5	-6.3	V	15 pF	1
H1L High Level	H1Lhigh	High	1.3	1.5	1.7			
RG Low Level	RGL	Low	0.3	0.5	0.7	V	21 pF	1
RG High Level	RGH	High	7.8	8.0	8.2			

Notes:
1. All pins draw less than 10 µA DC current. Capacitance values relative to SUB (substrate).
2. Clock capacitance is the effective capacitance extrapolated from the rise and fall time measured while operating the sensor.

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			24	MHz	1, 2
V1, V2 Clock Frequency	f_V			45.5	kHz	1, 2
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5		10	%	3, 7
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5		10	%	3
V1 - V2 Cross-over	V_{VCR}	1			V	
H1 - H2 Cross-over	V_{HCR}	-3.0	-1.5	0	V	
H1L Rise – H2 Fall Crossover	V_{H1LCR}	-2.0		1.0	V	9
H1, H2 Setup Time	t_{HS}	1	5		μs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	11			μs	2, 6
Flush clock off time	t_{off}	4			μs	2, 6
Pixel Period (1 Count)	t_e	42			ns	2
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	505			ms	6, 8
Integration Time	t_{int}		-			5, 6
Line Time	t_{line}	140			μs	6
Fast Flush Time	t_{flush}	88			ms	

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10 nsec whichever is greater based on the frequency of the horizontal clocks.
8. $t_{readout} = t_{line}$ * 3610 lines.
9. The charge capacity near the output could be degraded if the voltage at the clock cross over point is outside this range.

EDGE ALIGNMENT

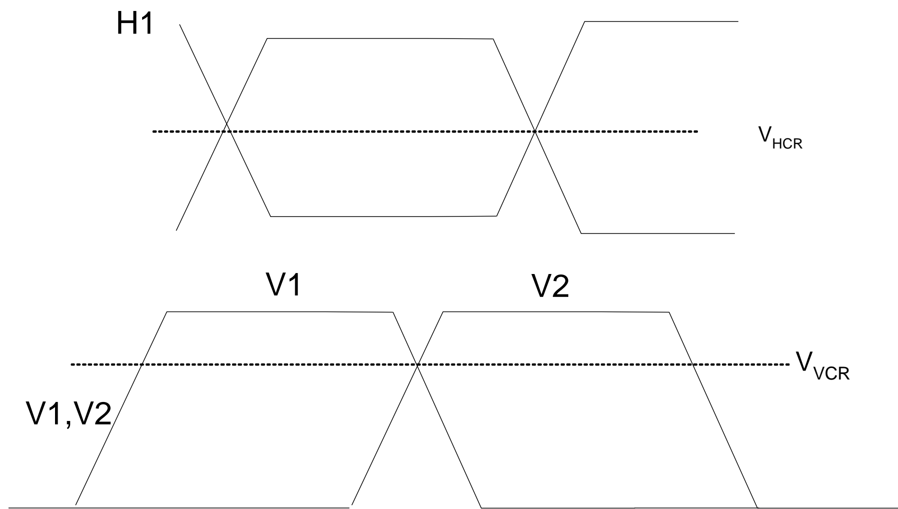


Figure 9: Timing Edge Alignment

FRAME TIMING

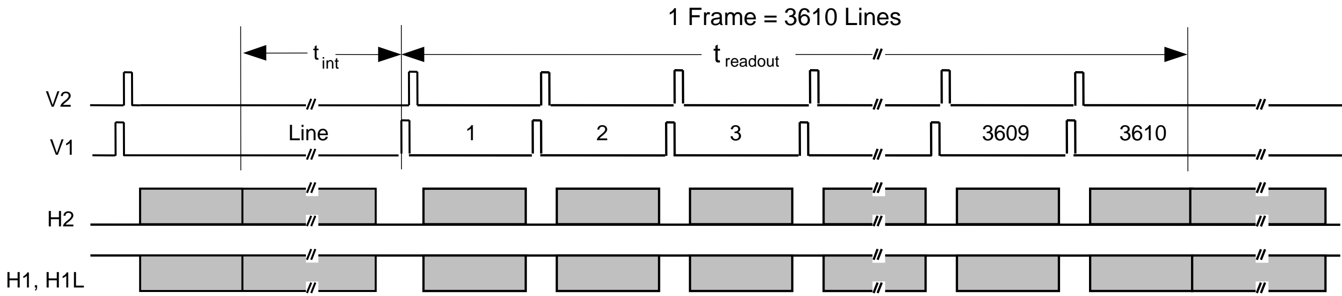


Figure 10: Frame Timing

Frame Timing Detail

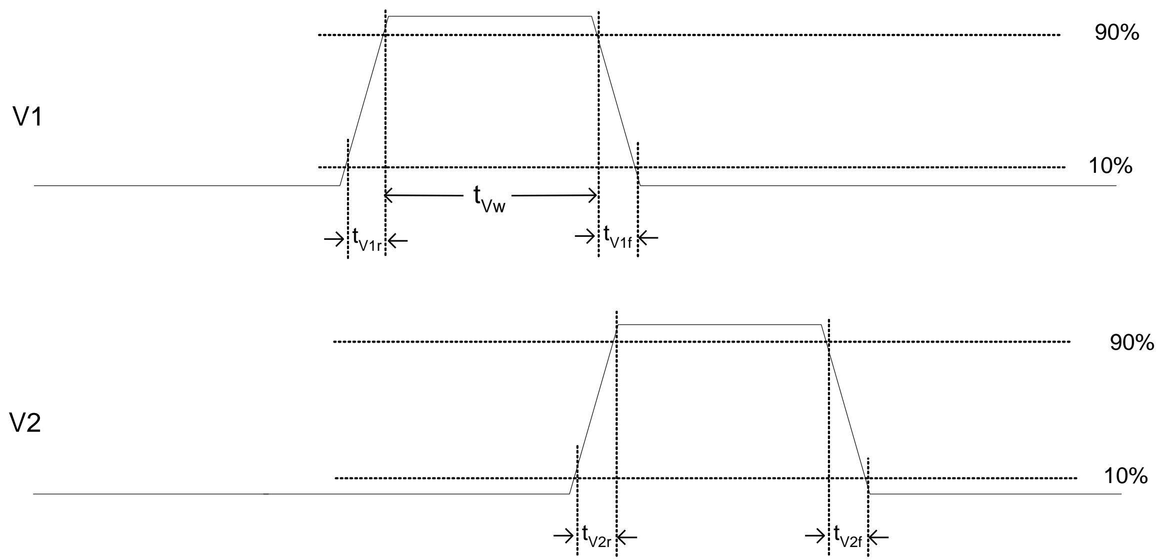


Figure 11: Frame Timing Detail

LINE TIMING (EACH OUTPUT)

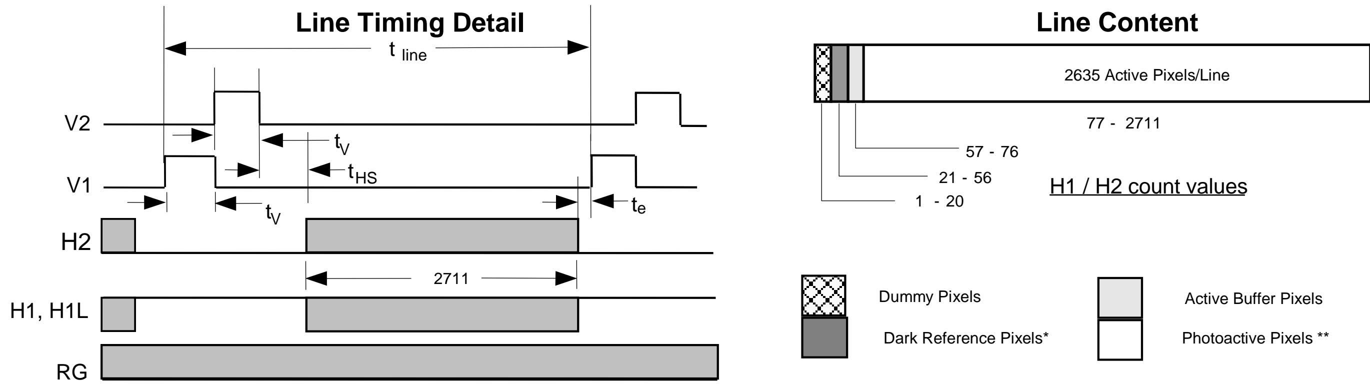


Figure 12: Line Timing

PIXEL TIMING

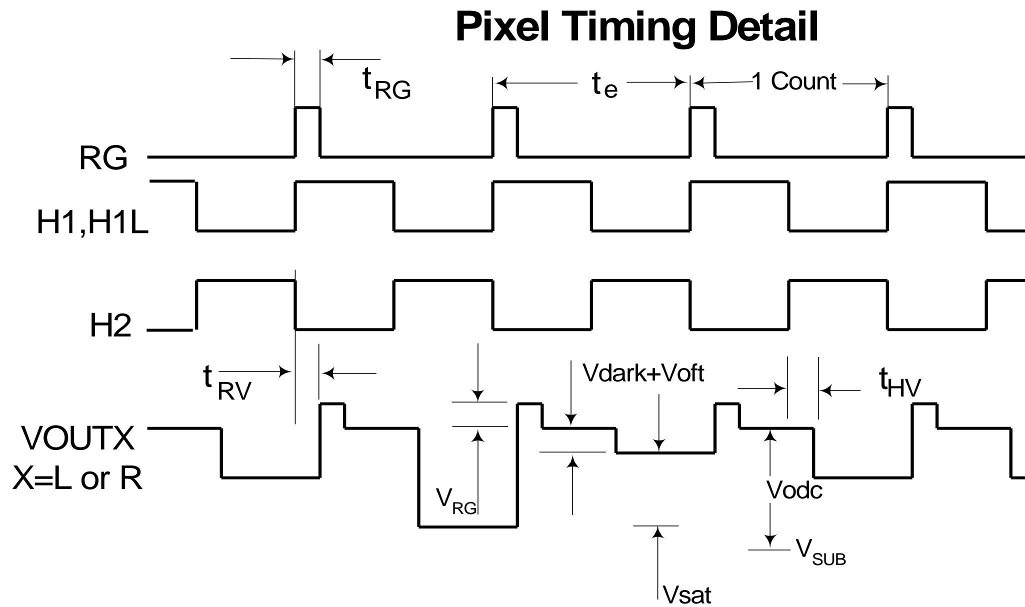


Figure 13: Pixel Timing

Pixel Timing Detail

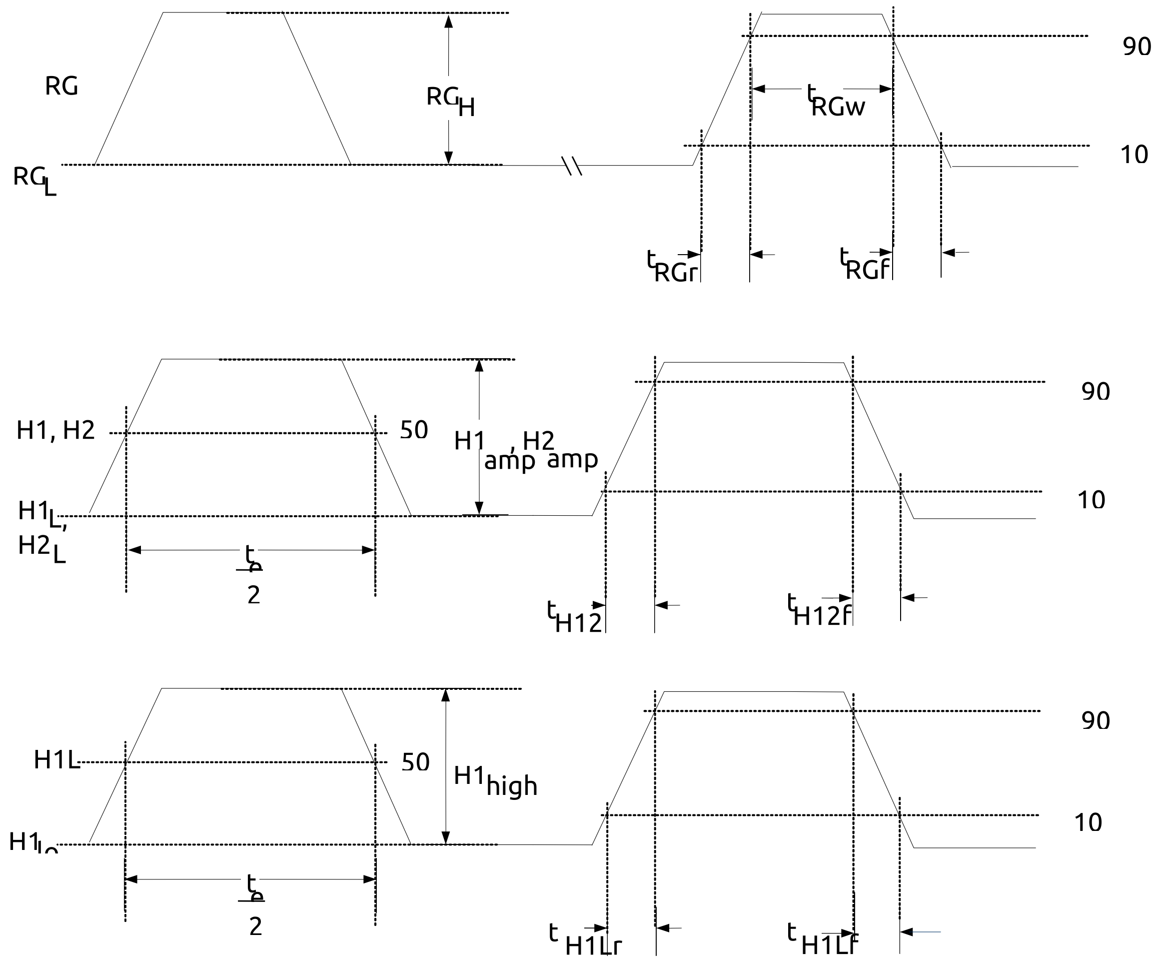


Figure 14: Pixel Timing Detail

MODE OF OPERATION

Power-up Flush Cycle

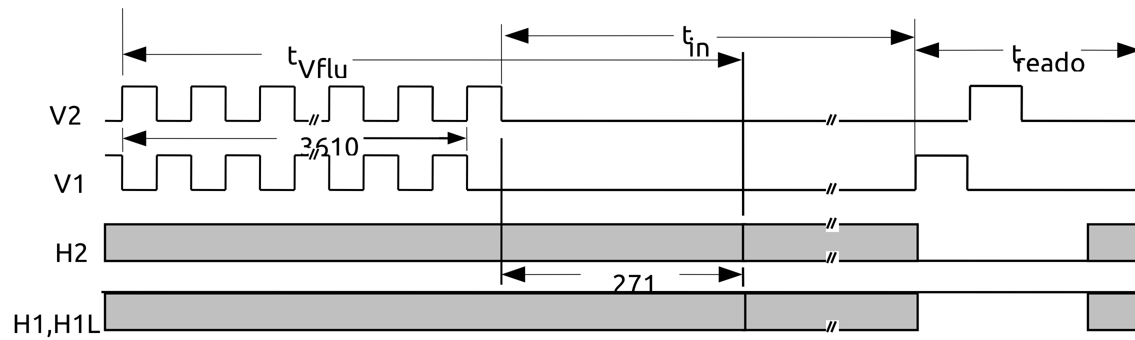


Figure 15: Power-up Flush Cycle

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1
Humidity	RH	5	70	%	2

Notes:
1. Long-term storage toward the maximum temperature will accelerate color.
2. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices.*

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions.*
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

Completed Assembly

NOTES:
1. ALL DIMENSIONS ARE DERIVED FROM PART MODEL FILE DATA BASE AND ORIGINATE FROM THE PRIMARY DATUM PLANES UNLESS OTHERWISE SPECIFIED.
2. BACK OF PACKAGE (ITEM 1) IS MARKED, APPROXIMATELY WHERE SHOWN (FONT SIZE 12 APPROX.).
3. DIE ADHESIVE IS APPLIED ON THE DIE ATTACH AREA (ITEM 1) APPROXIMATELY WHERE SHOWN. DISPENSE PATTERN AND AMOUNT OF EPOXY ARE SET BY ENGINEEER. ADHESIVE IS NOT SHOWN FOR CLARITY.
4. DIMENSION APPLIES FROM TOP OF DIE TO TOP OF WIRE (LOOP HEIGHT)
5. DIE PLACEMENT (ITEM 2) TO BE PARALLEL TO PACKAGE (ITEM 1) DATUM B & C, AND NOT TO EXCEED 0.5° OF ROTATION FROM CENTER OF PACKAGE.
6. COVER GLASS PLACEMENT (ITEM 4) NOT TO OVERHANG FROM OUTSIDE EDGES OF THE PACKAGE (ITEM 1)

Figure 16: Completed Assembly Drawing

Cover Glass Specification

MAR Coated-IR Absorbing Cover Glass

1. Dust/Scratch/Digs/Defects: 20 micron max
2. Substrate material: Schott S8612 whose performance is as published and specifications controlled by Schott, North America. The cover glass supplied for this device is as shown in Figure 16. Data supplied in the graph below is a typical transmission of the AR coated material at 0.8 mm thickness.

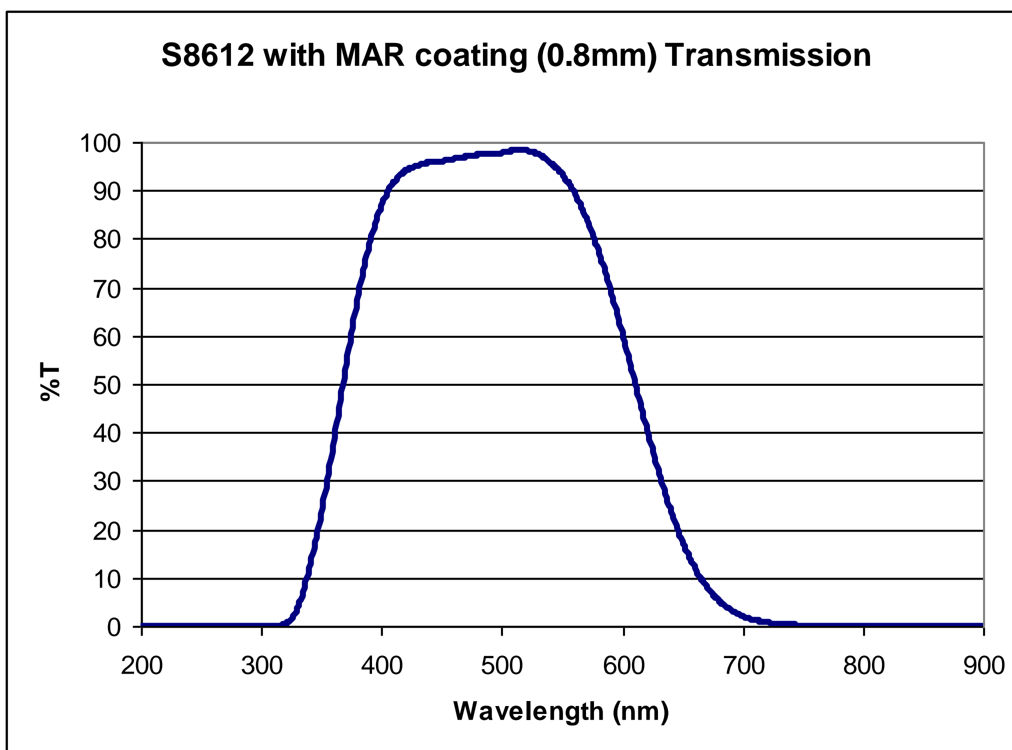


Figure 17: Cover Glass Substrate Transmission

3. Multilayer anti-reflective coating on two sides: Two-sided reflectance:

Wavelength	Transmission
420 – 450 nm	< 2 %
450 – 630 nm	< 1 %
630 – 680 nm	< 2 %

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

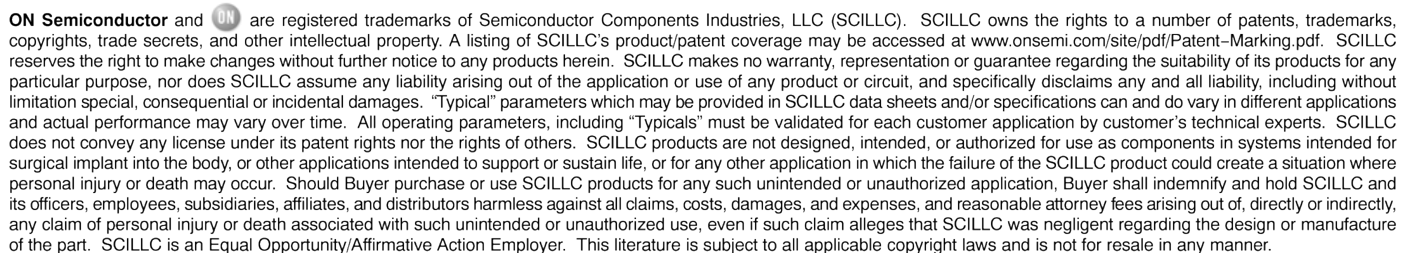
Revision Changes

MTD/PS-1412

Revision Number	Description of Changes
1.0	• Initial Release.

PS-0074

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template. • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections.
1.1	• Updated branding



ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

© 2014, Semiconductor Components Industries, LLC.